EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	53	703/22.ccls. and @pd>"20080101"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/02 10:58
L2	22	(golden adj reference) and (hdl or verilog or vhdl or rtl) and @ad<"20031001"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/02 11:09
L3	9	(pli or (program$4 adj language adj interface$1)) and (ISS or (instruction adj set adj simulat$5)) and (rtl or hdl or verilog or vhdl) and @ad<"20031001"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/07/02 11:13

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L4	1	((simulation adj design) and (reference adj value)).clm.	US-PGPUB	OR	OFF	2008/07/02 11:37
L5	0	((programming adj language adj interface) and (reference adj value)).clm.	US-PGPUB	OR	OFF	2008/07/02 11:38
L6	0	((PLI) and (reference adj value)).clm.	US-PGPUB	OR	OFF	2008/07/02 11:38

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... In the environment, **ISS** and **HDL** simulator communicate ... is built using the standard IPC library and the Verilog Program Language Interface(**PLI**) li- brary. ...
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... C' Instruction Set Simulators (**ISS**) fre- quently ... language" **VHDL** attributes (or **PLI** for Verilog). ... Comparatively to full **HDL** models, distributed models ...
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... built using the standard IPC library and the **Verilog** Program Language Interface(**PLI**) li- brary. ... tion for consistency checking from the **ISS** and adjusts ...
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... in "C" and implemented as a **PLI** code which is ... It is implemented as a **Verilog** stub which is ... the API to the target processor instruction set simulator (**ISS**). ...
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... and industry standard tools such as **Verilog** and VHDL ... generators, peripherals, and system memory through **PLI** calls ... **ISS** Coverage Coverage Target AVP+MVP RTPG VSG ...
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... Synchronization between different **verification** engines (netlist, RTL, or **ISS** simulators and ... **PLI** provides a mecha- nism to interface **Verilog** programs with ...
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... language using suitable interfaces such as **PLI**, VPI, FLI ... enhance the performance of the **ISS**, compiled code ... existing languages in academia, with **Verilog** and VHDL ...
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